AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor memory device, comprising:

a terminal group receiving an externally applied control signal, address, and data;

a memory cell array including a plurality of memory cells arranged in rows and columns; ~~transmitting/receiving said data to/from a region designated by said address in accordance with said control signal; and~~

B1

a logic circuit processing data in accordance with at least one of said control signal, said address, and said data when said address applied to said terminal group designates a prescribed first region of said memory cell array ~~if said control signal, address, and data are applied to said terminal group in a sequence of applying said control signal, address, and data to said memory cell array~~; and

a memory circuit transmitting/receiving said data to/from a memory cell corresponding to said address in said memory cells array in accordance with said control signal and said address when said address applied to said terminal group designates a region except said prescribed first region.

2. (Original) The semiconductor memory device according to claim 1, further comprising an interface portion receiving said control signal, said address, and said data from said terminal group for instructing an operation in accordance with at least one of said control signal, said address, and said data with respect to at least one of said memory cell array and said logic circuit in accordance with said address, said logic circuit including

B

a data holding portion for holding a content of the instruction from said interface portion, and

a data processing circuit for processing data according to the content held in said data holding portion.

3. (Original) The semiconductor memory device according to claim 2, wherein said instruction content includes a command for designating an operation of said data processing circuit, and input data processed by said data processing circuit, and

said holding portion includes

a first holding circuit holding said command,

a second holding circuit holding said input data, and

a third holding circuit holding a result of said data processing circuit resulting from said input data.

4. (Original) The semiconductor memory device according to claim 3, wherein said data holding portion further includes a fourth holding circuit holding a flag indicating as to if the data process has been completed by said data processing circuit.

5. (Original) The semiconductor memory device according to claim 3, wherein said data processing circuit performs an encryption process, and said input data includes key data of a cipher.

6. (Original) The semiconductor memory device according to claim 2, wherein said instruction content includes designation of a plurality of operation modes of said data processing circuit, and

said data holding portion has a holding circuit holding said plurality of operations modes, said holding circuit has a capacity of bits corresponding to data written to said memory array at a time, and

B1

the designation of said plurality of operation modes with respect to said logic circuit is performed in a sequence of one operation of writing data to said memory cell array.

7. (Original) The semiconductor memory device according to claim 2, wherein said interface portion includes a mode register which can be rewritten in accordance with said control signal, and

said interface portion determines a portion of an address space to which said first region is allocated in accordance with a value held in said mode register.

8. (Original) The semiconductor memory device according to claim 1, wherein said prescribed first region is a portion of a real address space of said memory cell array.

9. (Original) The semiconductor memory device according to claim 1, wherein said prescribed first region is a portion of a virtual address space other than a real address space of said memory cell array.

B

10. (Original) The semiconductor memory device according to claim 9, wherein said logic circuit processes data stored in said address space of said memory cell array corresponding to said prescribed first region in accordance with access to said prescribed first region which is a portion of said virtual address space.

B1

Claims 11-13 (Cancelled)

11
14. (Currently amended) A semiconductor memory device, comprising:

a first terminal group receiving an externally applied control signal, address, and data;

~~a second terminal receiving an externally applied select signal;~~

a memory including a plurality of memory cells arranged in rows and columns and activated in accordance with an externally applied ~~said~~ select signal for transmitting/receiving said data in accordance with said control signal with respect to a memory cell in a region designated by said address; ~~and~~

a logic circuit activated in accordance with said select signal in a complementary manner with respect to said memory for processing data in accordance with at least one of said address and said data; and

a second terminal receiving said select signal.

12 11
15. (Original) The semiconductor memory device according to claim 14, wherein said memory performs an operation of selecting said memory cell in accordance with said address including a row address and a column address time divisionally applied to said first terminal group, and

B

said logic circuit performs an operation in accordance with said address is collectively applied to said first terminal group.

B1

13 12

16. (Original) The semiconductor memory device according to claim 15, wherein said logic circuit includes an ATD circuit detecting changes in said row address and said column address for generating an operation timing.

B